Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A multiplication unit, comprising a 2N-bit multiplier and having a first short word length multiplication mode and a second long word length multiplication mode, wherein a short word length is N and a long word length is 2N, wherein N is an integer, and wherein:

in the first mode for multiplying two N-bit numbers, a first long word length multiplicand is formed from a first short word length multiplicand, a second long word length multiplicand is formed from a second short word length multiplicand, and the first and second long word length multiplicands are multiplied together using the 2N-bit multiplier to form a result which includes the product of the first and second short word length multiplicands, and

in the second mode for multiplying two 2N-bit numbers, wherein a third long word length multiplicand is formed from a first pair of short word length words and a fourth long word length multiplicand is formed from a second pair of short word length words, first words of the first and second pairs of short word length words are stored in respective registers connected to the 2N-bit multiplier, and subsequently the third and fourth long word length multiplicands are multiplied together using the 2N-bit multiplier.

2. (Original) A multiplication unit as claimed in claim 1, wherein:

in the first mode, the first long word length multiplicand is formed as a sign extended version of the first short word length multiplicand, and the second long word length multiplicand is formed as a sign extended version of the second short word length multiplicand.

3. (Original) A multiplication unit as claimed in claim 1, wherein:

in the first mode, the first long word length multiplicand is formed from the first short word length multiplicand plus zeroes as the most significant bits, and the second long word length multiplicand is formed from the second short word length multiplicand plus zeroes as the most significant bits, such that the multiplication result includes an unsigned product of the first and second short word length multiplicands.

4. (Original) A multiplication unit as claimed in claim 1, wherein:

in the first mode, the first long word length multiplicand is formed from the first short word length multiplicand plus zeroes as the least significant bits, and the second long word length multiplicand is formed from the second short word length multiplicand plus zeroes as the least significant bits, such that upper bits of the multiplication result contain the product of the first and second short word length multiplicands.

5. (Original) A multiplication unit as claimed in claim 1, wherein:

in the second mode, second words of the first and second pairs of short word length words are stored in respective registers, before the third and fourth long word length multiplicands are multiplied together.

6. (Original) A multiplication unit as claimed in claim 1, comprising a register file, from which the first and second short word length multiplicands, and the first and second pairs of short word length words, can be retrieved.

7. (Original) A multiplication unit as claimed in claim 6, wherein the register file is a dual ported register file, such that:

in the first mode, the first and second short word length multiplicands can be retrieved at the same time, and

in the second mode, first words of the first and second pairs of short word length words can be retrieved at a first time, and second words of the first and second pairs of short word length words can be retrieved at a second time.

8. (Original) A multiplication unit as claimed in claim 1, further comprising first and second long word length accumulators, for receiving the multiplication results.

9. (Original) A multiplication unit as claimed in claim 8, wherein, in the second mode, the result of multiplying together the third and fourth long word length multiplicands can be divided between the first and second long word length accumulators.

10. (Original) A multiplication unit as claimed in claim 8, wherein, in the second mode, a selected part of the result of multiplying together the third and fourth long word length multiplicands can be stored in a selected one of the first and second long word length accumulators.

11. (Original) A multiplication unit as claimed in claim 1, wherein the short word length is 16 bits and the long word length is 32 bits.

12. (Original) A multiplication unit as claimed in claim 1, wherein the short word length is 18 bits and the long word length is 36 bits.

13. (Original) A multiplication unit as claimed in claim 1, comprising a multiplier, for multiplying together the first and second short word length multiplicands in the first mode, and for multiplying together the third and fourth long word length multiplicands in the second mode, wherein:

in the first mode, the first long word length multiplicand is formed from the first short word length multiplicand plus zeroes as the most significant bits, and the second long word length multiplicand is formed from the second short word length multiplicand plus zeroes as the

most significant bits, and the multiplier is adapted to produce a signed product of the first and second short word length multiplicands as a multiplication result, and wherein:

in the second mode, the multiplier is adapted to produce a signed product of the third and fourth long word length multiplicands as a multiplication result.

14. (Currently Amended) A method of operating a multiplication unit, comprising a 2N-bit multiplier and having a first short word length multiplication mode and a second long word length multiplication mode, wherein a short word length is N and a long word length is 2N, wherein N is an integer, the method comprising:

in the first mode for multiplying two N-bit numbers, forming a first long word length multiplicand from a first short word length multiplicand, forming a second long word length multiplicand from a second short word length multiplicand, and using the 2N-bit multiplier to multiply ~~multiplying~~ together the first and second long word length multiplicands to form a result which includes the product of the first and second short word length multiplicands, and

in the second mode for multiplying two 2N-bit numbers, wherein a third long word length multiplicand is formed from a first pair of short word length words and a fourth long word length multiplicand is formed from a second pair of short word length words, storing first words of the first and second pairs of short word length words in respective registers connected to the 2N-bit multiplier, and subsequently multiplying together the third and fourth long word length multiplicands using the 2N-bit multiplier.

15. (Original) A method as claimed in claim 14, comprising:

in the first mode, forming the first long word length multiplicand as a sign extended version of the first short word length multiplicand, and forming the second long word length multiplicand as a sign extended version of the second short word length multiplicand.

16. (Original) A method as claimed in claim 14, comprising:

in the first mode, forming the first long word length multiplicand from the first short word length multiplicand plus zeroes as the most significant bits, and forming the second long word length multiplicand from the second short word length multiplicand plus zeroes as the most significant bits.

17. (Original) A method as claimed in claim 14, comprising:

in the first mode, forming the first long word length multiplicand from the first short word length multiplicand plus zeroes as the least significant bits, and forming the second long word length multiplicand from the second short word length multiplicand plus zeroes as the least significant bits.

18. (Original) A method as claimed in claim 14, comprising:

in the second mode, storing second words of the first and second pairs of short word length words in respective registers, before the third and fourth long word length multiplicands are multiplied together.

19. (Original) A method as claimed in claim 14, comprising retrieving the first and second short word length multiplicands, and the first and second pairs of short word length words, from a register file

20. (Original) A method as claimed in claim 19, wherein the register file is a dual ported register file, such that:

in the first mode, the first and second short word length multiplicands can be retrieved at the same time, and

in the second mode, first words of the first and second pairs of short word length words can be retrieved at a first time, and second words of the first and second pairs of short word length words can be retrieved at a second time.

21. (Original) A method as claimed in claim 14, further comprising selectively storing the multiplication results in first and second long word length accumulators.

22. (Original) A method as claimed in claim 21, comprising, in the second mode, dividing the result of multiplying together the third and fourth long word length multiplicands between the first and second long word length accumulators.

23. (Original) A method as claimed in claim 21, comprising, in the second mode, storing a selected part of the result of multiplying together the third and fourth long word length multiplicands in a selected one of the first and second long word length accumulators.

24. (Original) A method as claimed in claim 14, wherein the short word length is 16 bits and the long word length is 32 bits.

25. (Original) A method as claimed in claim 14, wherein the short word length is 18 bits and the long word length is 36 bits.

26. (Currently Amended) A multiplication unit~~,~~ comprising a register file which is adapted to store data words of a first length~~,~~ and a multiplier which is adapted to multiply together data words of a second length, wherein the second length is twice the first length,

wherein, in a first mode of operation for multiplying two words of the first length, first and second data words of the first length are retrieved from the register file and are converted to first and second data words of the second length, and the first and second data words of the second length are multiplied together in said multiplier, and

wherein, in a second mode of operation for multiplying two words of the second length, third and fourth data words of the first length are retrieved from the register file and are stored in respective multiplication registers, fifth and sixth data words of the first length are retrieved from the register file, the third and fifth data words of the first length are combined to

form a third data word of the second length, the fourth and sixth data words of the first length are combined to form a fourth data word of the second length, and the third and fourth data words of the second length are multiplied together in said multiplier.

27. (Original) A multiplication unit as claimed in claim 26, wherein, in the second mode of operation, the fifth and sixth data words of the first length are stored in respective multiplication registers after retrieval from the register file.

28. (Original) A multiplication unit as claimed in claim 26, further comprising first and second accumulators, each of at least the second length, for receiving the multiplication results from said multiplier.

29. (Original) A multiplication unit as claimed in claim 28, wherein, in the second mode, the result of multiplying together the third and fourth data words of the second length can be divided between the first and second accumulators.

30. (Original) A multiplication unit as claimed in claim 28, wherein, in the second mode, a selected part of the result of multiplying together the third and fourth data words of the second length can be stored in a selected one of the first and second accumulators.

31. (Original) A multiplication unit as claimed in claim 26, wherein the first length is 16 bits and the second length is 32 bits.

32. (Original) A multiplication unit as claimed in claim 26, wherein the first length is 18 bits and the second length is 36 bits.